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Total Number of Pages in This Submission

Application Number

10/811,191

Filing Date

03/26/2004

First Named Inventor

RUECKES, et al.

Art Unit

2818

Examiner Name

TBA

Attorney Docket Number

112020.147 US2 (NAN-23)

ENCLOSURES (Check all that apply)

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<input type="checkbox"/> Reply to Missing Parts/ Incomplete Application	<input type="checkbox"/> Remarks	
<input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	1. PTO Form 1449	
	2. <u>31</u> Publications	

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Wilmer Cutler Pickering Hale and Dorr LLP		
Signature			
Printed name	Peter M. Dichiaro		
Date	1/21/05	Reg. No.	38,005

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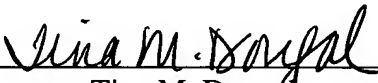
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: RUECKES, et al.
Application No.: 10/811,191 Examiner: To Be Assigned
Filed: March 26, 2004 Group Art Unit: 2818
For: Four Terminal Non-Volatile Transistor Device
Atty. Docket No.: 112020.147 US2 (NAN-23)

CERTIFICATE OF MAILING UNDER 37 CFR 1.8(a)

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INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants and their legal representatives hereby make of record on the attached Form PTO-1449 the following publications which are known to them and considered warranting disclosure under 37 C.F.R. §1.56 and 1.97-98.


Copies of the publications listed on the attached Form PTO-1449, with the exception of the cited U.S. Patents and the U.S. published applications, are submitted herewith. It is respectfully requested that the Examiner initial and return a copy of the subject Form PTO-1449 with the next Patent Office communication.

The submission of these publications does not constitute a representation by the Applicants that a search has been made or that no better art exists and does not constitute an admission that the listed publications are material or constitute "prior art." Applicants reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed publications, should one or more of the publications be applied against the claims of the present application.

As this paper is being filed prior to the issuance of a first Office Action on the merits, and pursuant to 37 C.F.R. § 1.97(b)(3), no fee is believed to be due. In the event a fee is due, the Commissioner is authorized to charge any fee deficiency or credit any overpayment to Deposit Account No. 08-0219.

Respectfully submitted,

Dated: January 21, 2005

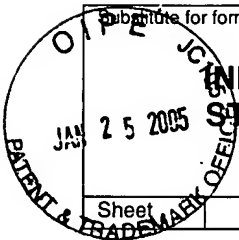


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Substitute for form 1449/PTO



INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 4

Complete if Known

Application Number	10/811,191
Filing Date	March 26, 2004
First Named Inventor	Rueckes, et al
Art Unit	2818
Examiner Name	TBA
Attorney Docket Number	112020.147US2 NAN-23

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-3,448,302	06-03-1969	SHANEFIELD	
		US-4,845,533	07-04-1989	PRYOR ET AL.	
		US-4,853,893	08-01-1989	EATON ET AL.	
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		US-2003/0124837	07/03/2003	RUECKES, et al.	
		US-2003/0165074A1	09-04-2003	SEGAL et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/811,191
				Filing Date	March 26, 2004
				First Named Inventor	Rueckes, et al
				Art Unit	2818
				Examiner Name	TBA
Sheet	2	of	4	Attorney Docket Number	112020.147US2 NAN-23

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		WO 01/44796 A1	06-21-2001	Board of Trustees of Leland Stanford Junior University	
		WO 01/03208 A1	01-11-2001	President and Fellows of Harvard College	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	A1	CHOI, W.B. et al., "Carbon-nanotube-based nonvolatile memory with oxide-nitride-film and nanoscale channel," <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(2), pp. 275-277.	
	A2	DEQUESNES, M. et al., "Calculation of pull-in voltages for carbon-nanotube-based nanoelectromechanical switches," <i>Nanotechnology</i> , 2002, Vol. 13, pp. 120-131.	
	A3	DEQUESNES, M. et al., "Simulation of carbon nanotube-based nanoelectromechanical switches," <i>Computational Nanoscience and Nanotechnology</i> , 2002, pp. 383-386.	
	A4	WOLF, S., Silicon Processing for the VLSI Era; Volume II – Manufacturing Yield and Reliability Issues of VLSI Interconnects, 1991, Lattice Press, Sunset Beach, pp. 260-273.	
	A5	WOLF, S., Multilevel-Interconnect Technology for VLSI and ULSI, 1990, Lattice Press, Sunset Beach, pp. 189-191.	
	A6	TOUR, J. M. et al., "NanoCell Electronic Memories," <i>J. Am. Chem Soc.</i> , 2003, Vol. 125, ppl 13279-13283.	

Examiner Signature	Date Considered
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Sheet	3	of	4	

A7	RUECKES, T., et al., "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing" <i>Science</i> , 2000, Vol. 289, pp. 94-97.	
A8	FAN, S. et al., "Carbon nanotube arrays on silicon substrates and their possible application," <i>Physica E</i> , 2000, Vol. 8, pp. 179-183.	
A9	ZHAN, W. et al., "Microelectrochemical Logic Circuits," <i>J. Am. Chem. Soc.</i> , 2003, Vol. 125, pp. 9934-9935.	
A10	SOH, H. T. et al., "Integrated nanotube circuits: Controlled growth and ohmic contacting of single-walled carbon nanotubes," <i>Appl. Phys. Lett.</i> , 1999, Vol. 75(5), pp. 627-629.	
A11	KINARET, J.M. et al., "A carbon-nanotube-based nanorelay", <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(8), pp. 1287-1289.	
A12	FRANKLIN, N. R. et al., "Integration of suspended carbon nanotube arrays into electronic devices and electromechanical systems," <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(5), pp. 913-915.	
A13	AVOURIS, Ph., "Carbon nanotube electronics," <i>Chem. Physics</i> , 2002, Vol. 281, pp. 429-445.	
A14	DAI, H. et al., "Controlled Chemical Routes to nanotube Architectures, Physics, and Devices," <i>J. Phys. Chem. B</i> , 1999, Vol. 103, pp. 111246-11255.	
A15	HOMMA, Y. et al., "Growth of Suspended Carbon Nanotubes Networks on 100-nm-scale Silicon Pillars," <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(12), pp. 2261-2263.	
A16	AJAYAN, P.M., et al., "Nanometre-size tubes of carbon," <i>Rep. Prog. Phys.</i> , 1997, Vol. 60, pp. 1025-1062.	
A17	SREEKUMAR, T.V., et al., "Single-wall Carbon Nanotube Films", <i>Chem. Mater.</i> 2003, Vol. 15, pp. 175-178.	
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A19	FUHRER, M.S. et al., "High-Mobility Nanotube Transistor Memory," <i>Nano Letters</i> , 2002, Vol. 2(7), pp. 755-759.	
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A22	FISCHER, J.E. et al., "Magnetically aligned single wall carbon nanotube films: Preferred orientation and anisotropic transport properties," <i>Journal of Appl. Phys.</i> , 2003, Vol. 93(4), pp. 2157-2163.	
A23	LEE, K.H. et al., "Control of growth orientation for carbon nanotubes," <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(3), pp. 448-450.	
A24	CASAVANT, M.J. et al., "Neat macroscopic membranes of aligned carbon nanotubes," <i>Journal of Appl. Phys.</i> , 2003, Vol. 93(4), pp. 2153-2156.	
A25	AMI, S. et al., "Logic gates and memory cells based on single C ₆₀ electromechanical transistors," <i>Nanotechnology</i> , 2001, Vol. 12, pp. 44-52.	
A26	DEHON, A., "Array-Based Architecture for FET-Based, Nanoscale Electronics," <i>IEEE Transactions on Nanotechnology</i> , 2003, Vol. 2(1), pp. 23-32.	

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Sheet	4	of	4	Attorney Docket Number	112020.147US2 NAN-23

	A27	TANS, S. et al., "Room-temperature based on a single carbon nanotube," <i>Nature</i> , 1998. Vol. 393, pp. 49-52.	
	A28	CUI, J.B. et al., "Carbon Nanotube Memory Devices of High Charge Storage Stability," <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(17), pp. 3260-3262.	
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